Advanced Research in Electrical and Electronic Engineering
Print ISSN: 2349-5804; Online ISSN: 2349-5812 Volume 2, Number 2 October-December (2014) pp. 130-135

http://www.krishisanskriti.org/areee.html

Harmonic-Current Restraint based Algorithm for Digital Differential Protection of Power Transformer and its application in Inrush Current and Fault analysis for Loaded Transformer

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Abstract: *Transformer is a very important and major component in power system. It finds a major use in various sectors. As a result, their protection is of great importance to assure stable and reliable operation of the whole system. A transformer will be provided with as much protection as is commensurate with its voltage and power rating and the importance of its application. Over-current protection in the form of fuses may be the only protection provided to a small 100 kVA, 11 kV/440 V distribution transformer. A 250 MVA, 15 kV/400 kV generator-transformer in a large thermal power station, on the other hand, may be provided with very elaborate protection. This may consist of percentage differential protection (with harmonic restraint), a protection against incipient faults and a protection against over-fluxing as primary protection. These will be backed up by the over-current protection. Since the terminals of a transformer are physically close together, it is an ideal candidate for application of the principle of differential protection which is one of most effective method for mitigating internal faults. In this digital technique which is based on Fast Fourier Transform (FFT) is implemented. It is preferred over Discrete Fourier Transform (DFT) since the former reduces the relay tripping time within 10ms which is in accordance with IEEE standard. This algorithm is built on the principle of harmonic-current restraint, where the magnetizing-inrush current is characterized by large harmonic components content that are not noticeably present in fault current.*
The various challenges have been faced while building this algorithm these are Current Mismatch caused by the transformation ratio and differing CT Ratios. Inrush Phenomena and Harmonic Content Availability with second harmonic component quantity in Over-Excitation Phenomena, Delta- Wye Transformation of Currents, Zero Sequence Elimination, LTC induced Mismatch, CT Saturation, and CT Tolerance, Switch and On to Fault concerns. However, the key characteristics of this algorithm is to identify between internal fault, external fault and inrush current and to generate a logic through amplitude and harmonic comparator in such a manner that relay must trip only in case of internal fault. The proposed digital differential relay is designed using a simulation technique in Matlab Simulink environment.

Index terms: OLTC-(on-load Tap changing Transformer, CT-(Current Transformer), CB-(Circuit Breakers)

1. INTRODUCTION

Differential protection of transformer involves establishing circulating current through a pair of matched CTs installed on the primary and secondary winding of the transformer. If there is no internal fault in the transformer, zero current flows through the differential overcurrent element. However, in case of an internal fault, the CT secondary currents are not matched and hence the differential current is not zero. This causes the overcurrent element to pick up and operate the circuit breakers to isolate the transformer.

Selection of CT Turns Ratio:
Let the transformer turns ratio given by N_1:N_2 and the corresponding CT ratio be given by1:n_1 and 1:$n_2$as given in fig 1. Then,
Current in CT-1 primary = I_1
Current in CT-1 secondary =$\frac{I_1}{n_1}$
Current in CT-2 primary =$\frac{N_1 I_1}{N_2}$
Current in CT-2 If there is no fault, then with proper connections account for the CT polarity, we should obtain circulatory current through CT secondary. Hence $i_1 = i_2$
Selection of CT Turns Ratio secondary=$\frac{N_1}{N_2}\frac{I_1}{n_2}$

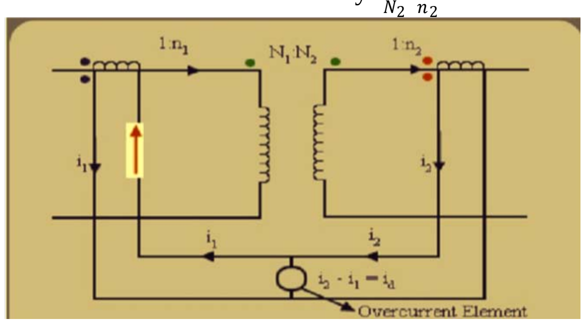

Fig. 1: Differential relay schematic diagram

If there is no fault, then with proper connections account .Selection of CT Turns Ratio i.e,$N_2\, n_2 = N_1 n_1$.If the transformer (to be protected) is working on tap T as shown in fig 2, then the above equality has to be modified as follows

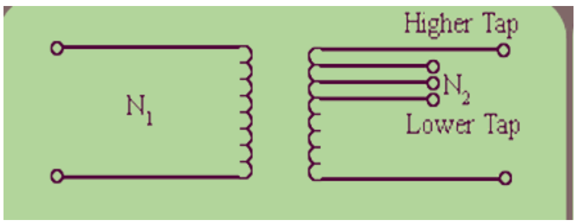

Fig. 2: Tap-changing transformer
$N_1 n_1 = N_2 n_2$T; condition for Tap changing Transformer

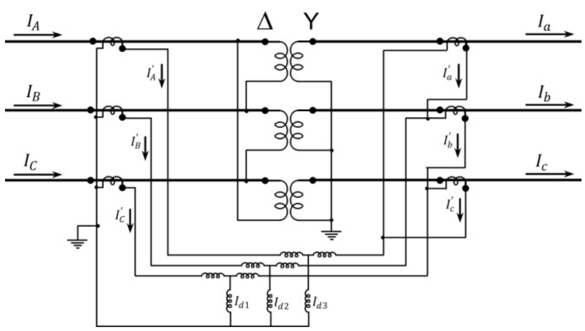

Fig. 3: $Y - \Delta$ *connected Transformer*

In some cases, of 3-φ power transformer connections as shown in Fig. 3, a 30° phase shift between primary and secondary currents is taking place. This phase shift occurs in the Y-Δ or Δ-Y connected transformers due to the transformation of the current from Y-Δ or Δ-Y as illustrated in the Fig. 3. This phase shift can be corrected easily by connecting the CTs secondary circuits in opposite way to the way that the power transformer phases are connected. I.e. if the transformer windings are connected in Y-Δ the CTs secondary windings should be connected in Δ-Y and vice versa [20]. As shown in Fig. 4 the relation between line-to-line voltage (V_{LL}) to the phase voltage (V_{ph}) can explain the phase shift between the Δ-Y transformer connection. The following equation gives the relationship between the line-to-line voltage (V_{LL}) to the phase voltage (V_{ph}) .These complications have been considered in order to make the differential relay working properly

1. Magnetizing inrush current during initial energization,
2. CTs Mismatch and saturation,
3. Transformation ratio changes of Tap changer.

1.1 Inrush current phenomenon

The major concern in power transformer protection is to avoid the false tripping of the protective relays due This phenomenon, the transient magnetizing inrush or the exciting current, occurs in the primary side of the transformer whenever the transformer is switched on (energized) and the instantaneous value of the voltage is not at 90°. At this time, the first peak of the flux wave is higher than the peak of the flux at the steady state condition.to misidentifying the magnetizing inrush current [1,2]. Magnetizing inrush currents may have a high magnitude, which is distinguishable from the traditional internal fault currents. To avoid needless trip by magnetizing inrush current, the second harmonic component is commonly used for blocking differential relay in power transformers. In general, the major sources of harmonics in the inrush currents are

a) Non-linearities of transformer core;
b) Saturation of current transformers;
c) Over-excitation of the transformers due to dynamic over voltage condition;
d) Core residual magnetization;
e) Switching instant

The transformer inrush current flows in one winding only. This results in large differential currents. Similarly, over excitation causes highly distorted differential current. But above cases are not fault conditions [5,6], therefore, the relay must be able to properly discriminate inrush and over excitation condition form internal fault condition. Under exciting inrush, the transformer response is featured by singular eruptions composed of high frequency elements of the reasons summarized above. There are many discrimination methods. Many conventional transformer protection methods employ the second harmonic restraint approach. Different algorithms such as discrete Fourier transform, least square methods, rectangular transforms, Walsh functions and Haar functions etc. are used to calculate the current harmonic contents.

1.2 False trip due to tap changer

On-Load Tap-Changer (OLTC) is installed on the power transformer to control automatically the transformer output voltage. This device is required wherever there are heavy fluctuations in the power system voltage. The transformation ratio of the CTs can be matched with only one point of the tap-changing range. Therefore, if the OLTC is changed, unbalance current flows in the differential relay operating coil.

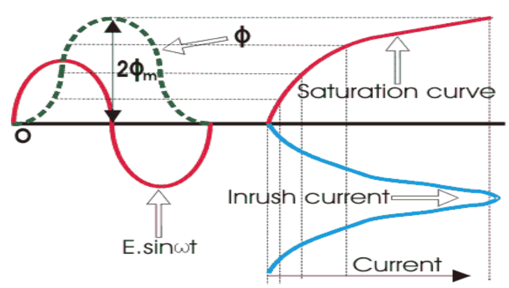

Fig. 4: Inrush current in Transformers

This action causes CTs mismatches. This current will be considered as a fault current which makes the relay to release a trip signal

1.3 False trip due to C.T characteristics

The performance of the differential relays depends on the accuracy of the CTs in reproducing their primary currents in their secondary side. In many cases, the primary ratings of the CTs, located in the high voltage and low voltage sides of the power transformer, does not exactly match the power transformer rated currents. Due to this discrepancy, a CTs mismatch takes place, which in turn creates a small false differential current, depending on the amount of this mismatch. Sometimes, this amount of the differential current is enough to operate the differential relay [9,10]. Therefore, CTs ratio correction has to be done to overcome this CTs mismatch by using interposing CTs of multi taps .Another problem that may face the perfect operation of the CTs is the saturation problem.

When saturation happens to one or all CTs at different levels, false differential current appears in the differential relay. This differential current could cause mal-operation of the differential relay. The dc component of the primary side current could produce the worst case of CT saturation. In which, the secondary current contains dc offset and extra harmonics.

2. ALGORITHM

The software is implemented according to the following steps

Step 1. Reading data from the CTs
Step 2. Data calculation, which is given as follows;
For the amplitude calculation, if the absolute difference between the output differential currents is greater than zero the logic (1) takes place, which indicates the case of an inrush current or an internal fault. Otherwise, the logic (0) takes place, which indicates a detection of an external fault.

In the meantime, the harmonic calculation is performed. If the percentage value of the second harmonic amplitude is in the range of (0.3 to 0.6) of the fundamental component amplitude, then the logic (0) occurs, that means recognition of inrush current. Otherwise, the logic (1) takes place, which indicates a detection of an internal or external fault.

Step 3. Taking the final decision:

If the logic cases received from both cases (a & b) in step two are both (1), that indicates a detection of an internal fault. Then a trip signal is released to stop the simulation. For the other logic options of (0,1) means an external fault, (1,0) means an inrush current, or (0,0) indicate an occurrence of an inrush current or an external fault, and the simulation goes back to step two to start the calculation again for the next sample. So amplitude comparator and harmonic comparator will respond in following manner

Amplitude comparator

If Amplitude comparator satisfies the following condition then it will give:
$|I_{d1} - I_{d2} > 0|$
It leads to logic 1 which indicate inrush current or internal fault.
$|I_{d1} - I_{d2} = 0|$
It leads to logic 0 which indicates external fault

Harmonic comparator
If harmonic comparator lead to following condition then it will give:
0.3F1<F2<0.7F1
It leads to logic 0, which means inrush current
If F2<0.3F1
It leads to logic 1, which means internal or external fault
From the above data, the truth table for the following operation can be described as:

Amplitude comparator output	Harmonic Comparator output	Action	Tripping of relay
0	0	Inrush Current or External Fault	No
0	1	External Fault	No
1	0	Inrush Current	No
1	1	Internal Fault	Yes

Fig. 4: Logic-table for Differential Relay

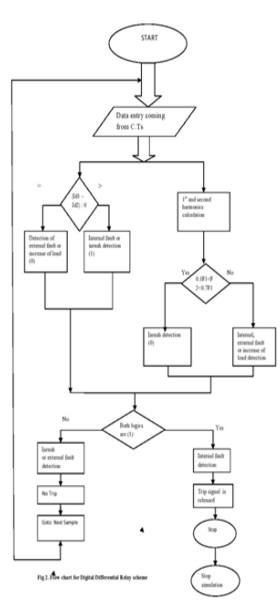

Fig. 5: Flowchart for following scheme

3. SYSTEM.DESCRIPTION

The implementation is done using Matlab/Simulink environment. Fig. 7 shows the simulated power system built in Matlab/Simulink environment. In which a three phase, 450MVA, 50Hz, (935/400) kV, Y/Δpower transformer is used in this system. Back to step two to start the calculation again for the next sample. The following algorithm is described in fig 5

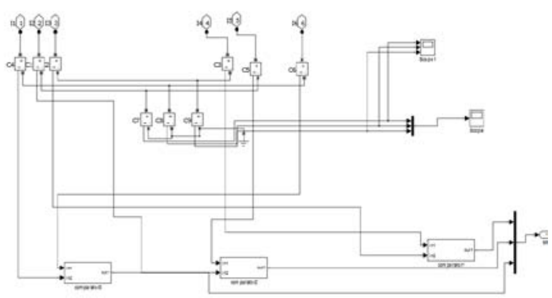

Fig. 6: Differential relay subsystem

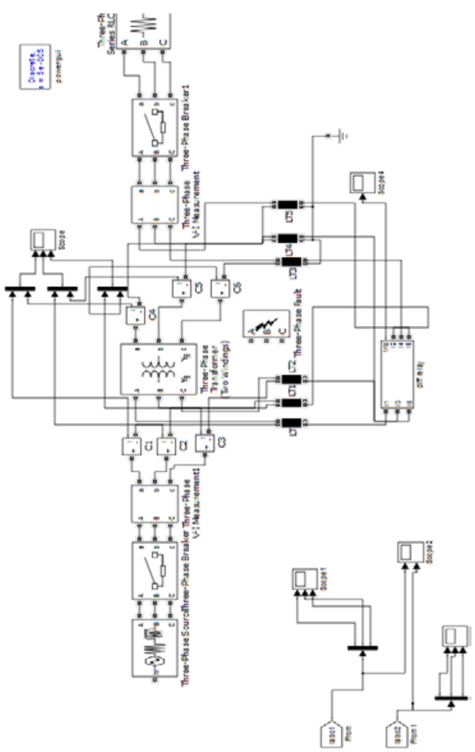

Fig. 7: Main Simulink Diagram

4. SIMULATIONS AND RESULTS

Case 1: Magnetizing inrush with adding load

This test is carried out after the energization of the power transformer by switching ON the CB1 at 0.1sec and CB2 at 0.3 sec from the beginning of the simulation to see the effect of load excursion on the accuracy of the designed approach. Therefore, a 500W resistive load is added to the system at 0.3 sec. Consequently, the inrush current disappeared and load current started to flow in the primary and secondary circuits of the transformer according to the transformation ratio of the power transformer as shown in Fig.10. However, the amplitude of the output currents of the primary and secondary CTs are equal due to the proper selection of the transformation ratio of the primary and secondary CTs, which can obviously noticed in Fig.9 . Where, before the time 0.3 sec the differential current was equal to the inrush current, but after the switching ON of the load the differential current went to zero and the primary and secondary currents became equal. As shown in Fig., after the switching of CB2, the value of the 2nd harmonic become lower than 0.3 of the fundamental component.

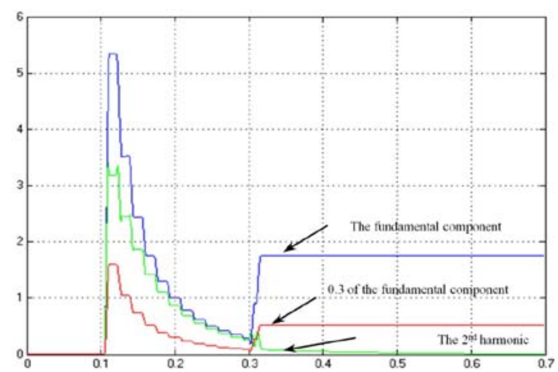

Fig. 8: 2nd harmonic and the fundamental component for the 1st case

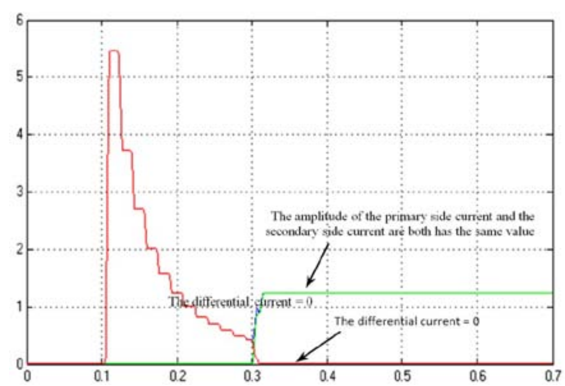

Fig. 9: Amplitude comparator results for the 1st case

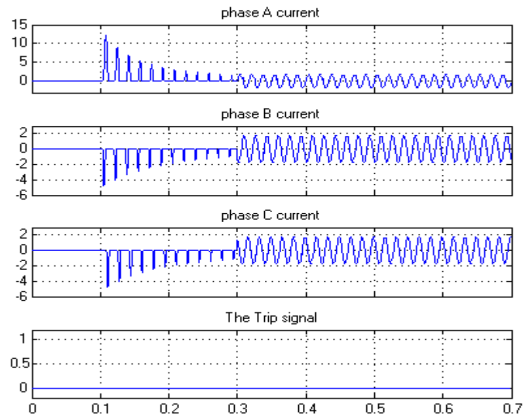

Fig. 10: Normal load current starts flowing at 0.3sec

Accordingly, the harmonic calculation part released logic (1) but the amplitude comparator released logic (0). Consequently, for this logic coordination (1,0) no trip signal is released. Fig. shows the amplitude comparator results.

Case 2: Three phase to ground fault at loaded transformer

In this section, a three phase to ground fault is created to test the security of the algorithm. After the switching of CB1 at 0.1sec, an internal fault is created at 0.5 sec at the secondary side of the power transformer by connecting the three phases A, B and C of the secondary side of the power transformer to the ground. In this case, a significant increase of the Primary current takes place due to the fault occurrence inside the protected zone at 0.5 sec as shown in Fig. 13. The relay detected this increase using the harmonic and amplitude comparators and realized it as an internal fault. Consequently the transformer is isolated from the grid.

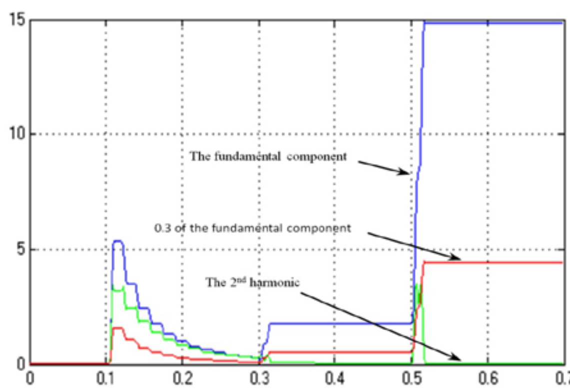

Fig. 11: 2nd harmonic and the fundamental component for the case of three-phase to ground fault at Loaded transformer.

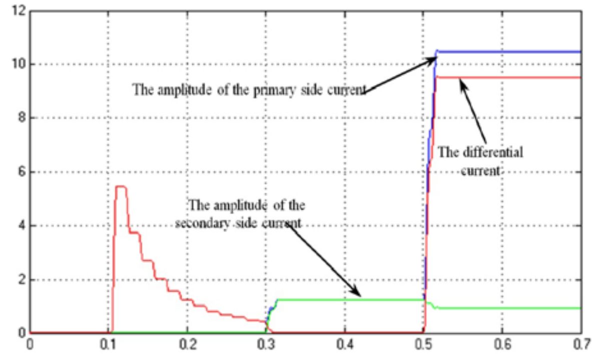

Fig. 12: Amplitude comparator result for the 2nd case.

Also it is obvious from Fig13 that the relay has released a trip signal after 0.57 msec after the occurrence of the fault, which can be considered as a very good speed to isolate the transformer. As shown in Fig.11 after the occurrence of the fault at time 0.5 sec, the value of the 2nd harmonic increased during the transient time and then decreased rapidly to a value lower than 0.3 of the fundamental component once the steady state is achieved. Accordingly, the harmonic calculation part released logic (1). Also from Fig. 12 which shows the result of the amplitude comparator the value of the differential current is no longer equal to zero. Accordingly the amplitude comparator released logic (1). Therefore, for this logic coordination (1,1) a trip signal is released in order to isolate the power transformer from the grid

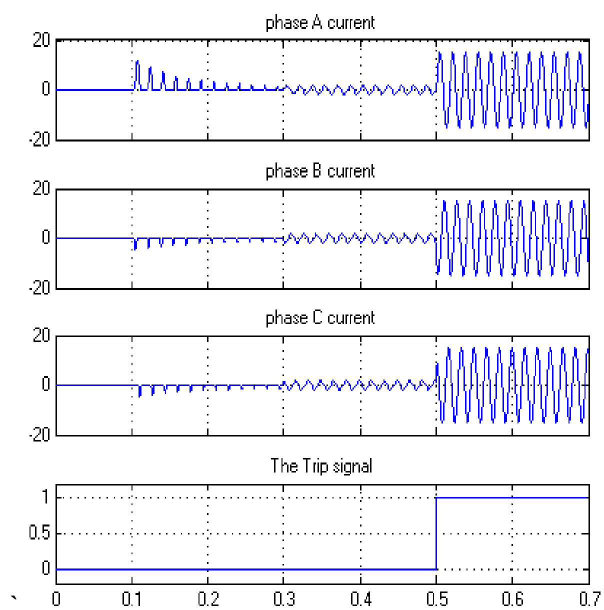

Fig. 13: Increase of phase A, B & C currents due to the occurrence of the fault at 0.5 sec for loaded Transformer.

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